CY29351

2.5V or 3.3V, 200 MHz, 9-Output Zero Delay Buffer

Features

- Output Frequency Range: 25 MHz to 200 MHz
- Input Frequency Range: 25 MHz to 200 MHz
- 2.5V or 3.3V Operation
- Split 2.5V and 3.3V Outputs
- ±2.5% Max Output Duty Cycle Variation
- Nine Clock Outputs: Drive up to 18 Clock Lines
- Two Reference Clock Inputs: LVPECL or LVCMOS
- 150-ps Max Output-Output Skew
- Phase-locked Loop (PLL) Bypass Mode
- Spread Aware
- Output Enable or Disable
- Pin-compatible with MPC9351
- Industrial Temperature Range: –40°C to +85°C
- 32-pin 1.0-mm TQFP Package

Functional Description

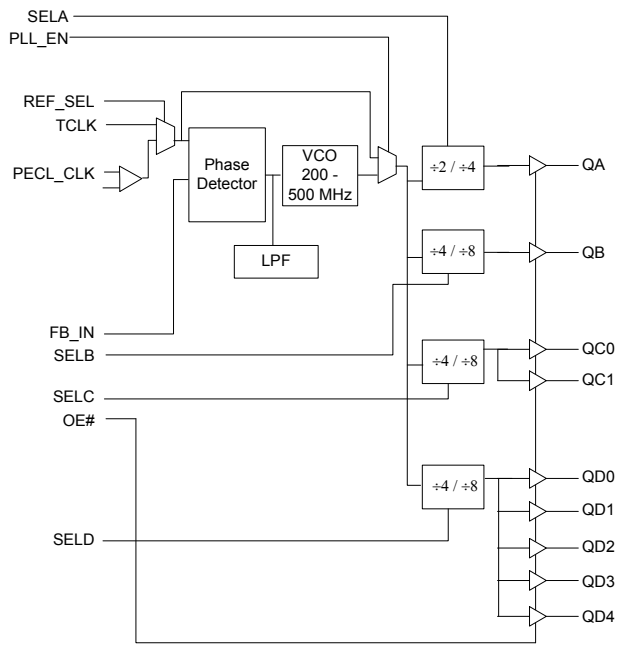
The CY29351 is a low voltage high performance 200 MHz PLL-based zero delay buffer designed for high speed clock distribution applications.

The CY29351 features LVPECL and LVCMOS reference clock inputs and provides nine outputs partitioned in four banks of one, one, two, and five outputs. Bank A divides the VCO output by two or four while the other banks divide by four or eight per SEL(A:D) settings (Table 3, “Function Table,” on page 3). These dividers enable output to input ratios of 4:1, 2:1, 1:1, 1:2, and 1:4. Each LVCMOS compatible output can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:18.

The PLL is ensured stable given that the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 25 MHz to 200 MHz. For normal operation, the external feedback input, FB_IN, is connected to one of the outputs. The internal VCO is running at multiples of the input reference clock set by the feedback divider (Table 2, “Frequency Table,” on page 3).

When PLL_EN# is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

Logic Block Diagram



Pinout

Figure 1. Pin Diagram - 32-Pin TQFP Package

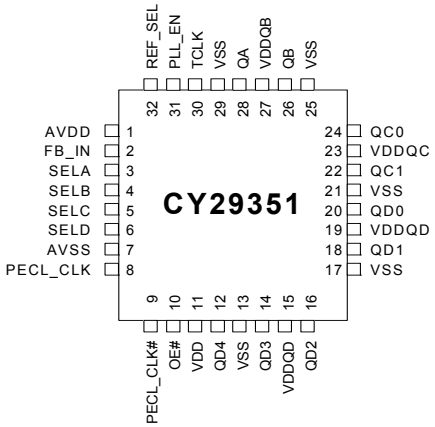


Table 1. Pin Definitions - 32-Pin TQFP Package

Pin[1]	Name	I/O	Type	Description
8	PECL_CLK	I, PU	LVPECL	LVPECL reference clock input
9	PECL_CLK#	I, PU/PD	LVPECL	LVPECL reference clock input. Weak pull up to VDD/2.
30	TCLK	I, PD	LVCMOS	LVCMOS/LVTTL reference clock input
28	QA	O	LVCMOS	Clock output bank A
26	QB	O	LVCMOS	Clock output bank B
22, 24	QC(1,0)	O	LVCMOS	Clock output bank C
12, 14, 16, 18, 20	QD(4:0)	O	LVCMOS	Clock output bank D
2	FB_IN	I, PD	LVCMOS	Feedback clock input. Connect to an output for normal operation. This input should be at the same voltage rail as input reference clock
10	OE#	I, PD	LVCMOS	Output enable/disable input
31	PLL_EN	I, PU	LVCMOS	PLL enable/disable input
32	REF_SEL	I, PD	LVCMOS	Reference select input
3, 4, 5, 6	SEL(A:D)	I, PD	LVCMOS	Frequency select input, bank (A:D)
27	VDDQB	Supply	VDD	2.5V or 3.3V power supply for bank B output clock[2,3]
23	VDDQC	Supply	VDD	2.5V or 3.3V power supply for bank C output clocks[2,3]
15, 19	VDDQD	Supply	VDD	2.5V or 3.3V power supply for bank D output clocks[2,3]
1	AVDD	Supply	VDD	2.5V or 3.3V power supply for PLL[4,5]
11	VDD	Supply	VDD	2.5V or 3.3V power supply for core, inputs, and bank A output clock[2,3]
7	AVSS	Supply	Ground	Analog ground
13, 17, 21, 25, 29	VSS	Supply	Ground	Common ground

Notes
1. PU = Internal pull up, PD = Internal pull down.
2. A 0.1-µF bypass capacitor should be placed as close as possible to each positive power pin (<0.2”). If these bypass capacitors are not close to the pins, the high-frequency filtering characteristics are cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQB, VDDQC, and VDDQD power supply pins.
4. Driving one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50 Ω series terminated transmission lines.
5. Inputs have pull up or pull down resistors that affect the input current.

Table 2. Frequency Table

Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
÷2	Input Clock * 2	100 MHz to 200 MHz	100 MHz to 190 MHz
÷4	Input Clock * 4	50 MHz to 125 MHz	50 MHz to 95 MHz
÷8	Input Clock * 8	25 MHz to 62.5 MHz	25 MHz to 47.5 MHz

Table 3. Function Table

Control	Default	0	1
REF_SEL	0	PCLK	TCLK
PLL_EN	1	Bypass mode, PLL disabled. The input clock connects to the output dividers	PLL enabled. The VCO output connects to the output dividers
OE#	0	Outputs enabled	Outputs disabled (three-state), VCO running at its minimum frequency
SELA	0	÷ 2 (bank A)	÷ 4 (bank A)
SELB	0	÷ 4 (bank B)	÷ 8 (bank B)
SELC	0	÷ 4 (bank C)	÷ 8 (bank C)
SELD	0	÷ 4 (bank D)	÷ 8 (bank D)

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	DC supply voltage		–0.3	5.5	V
V_{DD}	DC operating voltage	Functional	2.375	3.465	V
V_{IN}	DC input voltage	Relative to V_{SS}	–0.3	V_{DD} + 0.3	V
V_{OUT}	DC output voltage	Relative to V_{SS}	–0.3	V_{DD} + 0.3	V
V_{TT}	Output termination voltage		–	V_{DD} ÷ 2	V
LU	Latch-up immunity	Functional	200	–	mA
R_{PS}	Power supply ripple	Ripple frequency < 100 kHz	–	150	mVp-p
T_S	Temperature, storage	Non Functional	–65	+150	°C
T_A	Temperature, operating ambient	Functional	–40	+85	°C
T_J	Temperature, junction	Functional	–	+150	°C
$Ø_{JC}$	Dissipation, junction to case	Functional	42		°C/W
$Ø_{JA}$	Dissipation, junction to ambient	Functional	105		°C/W
ESD_H	ESD protection (human body model)		2000	–	Volts
FIT	Failure in time	Manufacturing test	10		ppm

DC Electrical Specifications

(V_{DD} = 2.5V ± 5%, T_A = –40°C to +85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input voltage, low	LVCMOS	–	–	0.7	V
V_{IH}	Input voltage, high	LVCMOS	1.7	–	V_{DD}+0.3	V
V_{PP}	Peak-Peak input voltage	LVPECL	250	–	1000	mV
V_{CMR}	Common mode range[6]	LVPECL	1.0	–	V_{DD} – 0.6	V
V_{OL}	Output voltage, low[4]	I_{OL} = 15mA	–	–	0.6	V
V_{OH}	Output voltage, high[4]	I_{OH} = –15mA	1.8	–	–	V
I_{IL}	Input current, low[5]	V_{IL} = V_{SS}	–	–	–100	µA
I_{IH}	Input current, high[5]	V_{IL} = V_{DD}	–	–	100	µA
I_{DDA}	PLL supply current	AVDD only	–	5	10	mA
I_{DDQ}	Quiescent supply current	All V_{DD} pins except AVDD	–	–	7	mA
I_{DD}	Dynamic supply current	Outputs loaded at 100 MHz	–	180	–	mA
		Outputs loaded at 200 MHz	–	210	–	
C_{IN}	Input pin capacitance		–	4	–	pF
Z_{OUT}	Output impedance		14	18	22	Ω

DC Electrical Specifications

(V_{DD} = 3.3V ± 5%, T_A = –40°C to +85°C)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IL}	Input voltage, low	LVCMOS	–	–	0.8	V
V_{IH}	Input voltage, high	LVCMOS	2.0	–	V_{DD} + 0.3	V
V_{PP}	Peak-Peak input voltage	LVPECL	250	–	1000	mV
V_{CMR}	Common mode range[6]	LVPECL	1.0	–	V_{DD} – 0.6	V
V_{OL}	Output Voltage, Low[4]	I_{OL} = 24 mA	–	–	0.55	V
		I_{OL} = 12 mA	–	–	0.30	
V_{OH}	Output voltage, high[4]	I_{OH} = –24 mA	2.4	–	–	V
I_{IL}	Input current, low[5]	V_{IL} = V_{SS}	–	–	–100	µA
I_{IH}	Input current, high[5]	V_{IL} = V_{DD}	–	–	100	µA
I_{DDA}	PLL supply current	AVDD only	–	5	10	mA
I_{DDQ}	Quiescent supply current	All VDD pins except AVDD	–	–	7	mA
I_{DD}	Dynamic supply current	Outputs loaded at 100 MHz	–	270	–	mA
		Outputs loaded at 200 MHz	–	300	–	
C_{IN}	Input pin capacitance		–	4	–	pF
Z_{OUT}	Output impedance		12	15	18	Ω

Note

6. V_{CMR} (DC) is the crossing point of the differential input signal. Normal operation is obtained when the crossing point is within the V_{CMR} range and the input swing is within the V_{PP} (DC) specification.

AC Electrical Specifications

(V_{DD} = 2.5V ± 5%, T_A = –40°C to +85°C)[7]

Parameter	Description	Condition	Min	Typ	Max	Unit
f_{VCO}	VCO frequency		200	–	380	MHz
f_{in}	Input frequency	÷2 feedback	100	–	190	MHz
		÷4 feedback	50	–	95	
		÷8 feedback	25	–	47.5	
		Bypass mode (PLL_EN = 0)	0	–	200	
f_{refDC}	Input duty cycle		25	–	75	%
V_{PP}	Peak-Peak input voltage	LVPECL	500	–	1000	mV
V_{CMR}	Common mode range[8]	LVPECL	1.2	–	V_{DD} – 0.6	V
t_r , t_f	TCLK input rise/fall time	0.7V to 1.7V	–	–	1.0	ns
f_{MAX}	Maximum output frequency	÷2 output	100	–	190	MHz
		÷4 output	50	–	95	
		÷8 output	25	–	47.5	
DC	Output duty cycle	f_{MAX} < 100 MHz	47.5	–	52.5	%
		f_{MAX} > 100 MHz	45	–	55	
t_r , t_f	Output rise/fall times	0.6V to 1.8V	0.1	–	1.0	ns
$t_{(\phi)}$	Propagation delay (static phase offset)	TCLK to FB_IN	–100	–	100	ps
		PCLK to FB_IN	–100	–	100	
$t_{sk(O)}$	Output-to-Output skew		–	–	150	ps
$t_{PLZ, HZ}$	Output disable time		–	–	10	ns
$t_{PZL, ZH}$	Output enable time		–	–	10	ns
BW	PLL closed loop bandwidth (–3dB)	÷2 feedback	–	2.2	–	MHz
		÷4 feedback	–	0.85	–	
		÷8 feedback	–	0.6	–	
$t_{JIT(CC)}$	Cycle-to-Cycle jitter	Same frequency	–	–	150	ps
		Multiple frequencies	–	–	250	
$t_{JIT(PER)}$	Period jitter	Same frequency	–	–	100	ps
		Multiple frequencies	–	–	175	
$t_{JIT(\phi)}$	I/O phase jitter		–	175	–	ps
t_{LOCK}	Maximum PLL lock time		–	–	1	ms

Notes
7. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Parameters are guaranteed by characterization and are not 100% tested.
8. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset t(ϕ).

AC Electrical Specifications

(V_{DD} = 3.3V ± 5%, T_A = –40°C to +85°C)[7]

Parameter	Description	Condition	Min	Typ.	Max	Unit
f_{VCO}	VCO frequency		200	–	500	MHz
f_{in}	Input frequency	÷2 feedback	100	–	200	MHz
		÷4 feedback	50	–	125	
		÷8 feedback	25	–	62.5	
		Bypass mode (PLL_EN = 0)	0	–	200	
f_{refDC}	Input duty cycle		25	–	75	%
V_{PP}	Peak-Peak input voltage	LVPECL	500	–	1000	mV
V_{CMR}	Common mode range[8]	LVPECL	1.2	–	V_{DD} – 0.9	V
t_r , t_f	TCLK input rise/fall time	0.8V to 2.0V	–	–	1.0	ns
f_{MAX}	Maximum output frequency	÷2 output	100	–	200	MHz
		÷4 output	50	–	125	
		÷8 output	25	–	62.5	
DC	Output duty cycle	f_{MAX} < 100 MHz	47.5	–	52.5	%
		f_{MAX} > 100 MHz	45	–	55	
t_r , t_f	Output rise/fall times	0.8V to 2.4V	0.1	–	1.0	ns
$t_{(\phi)}$	Propagation delay (static phase offset)	TCLK to FB_IN, same VDD	–100	–	100	ps
		PCLK to FB_IN, same VDD	–100	–	100	
$t_{sk(O)}$	Output-to-Output skew	Banks at same voltage	–	–	150	ps
tsk(B)	Bank-to-Bank skew	Banks at different voltages	–	–	350	ps
$t_{PLZ, HZ}$	Output disable time		–	–	10	ns
$t_{PZL, ZH}$	Output enable time		–	–	10	ns
BW	PLL closed loop bandwidth (–3dB)	÷2 feedback	–	2.2	–	MHz
		÷4 feedback	–	0.85	–	
		÷8 feedback	–	0.6	–	
$t_{JIT(CC)}$	Cycle-to-Cycle jitter	Same frequency	–	–	150	ps
		Multiple frequencies	–	–	250	
$t_{JIT(PER)}$	Period jitter	Same frequency	–	–	100	ps
		Multiple frequencies	–	–	150	
$t_{JIT(\phi)}$	I/O phase jitter	I/O same V_{DD}	–	175	–	ps
t_{LOCK}	Maximum PLL lock time		–	–	1	ms

Figure 2. LVCMOS_CLK AC Test Reference for V_{DD} = 3.3V / 2.5V

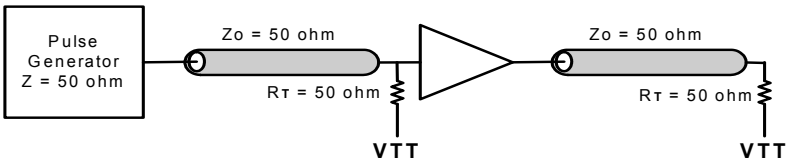


Figure 3. PECL_CLK AC Test Reference for V_{DD} = 3.3V / 2.5V

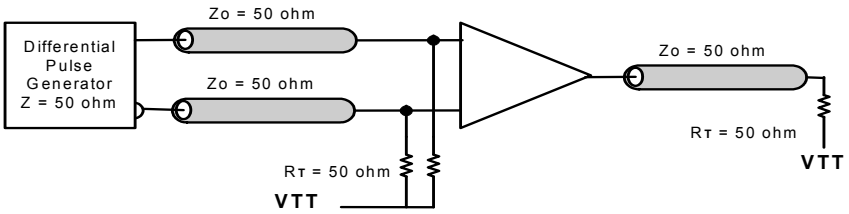


Figure 4. LVPECL Propagation Delay t(f), Static Phase Offset

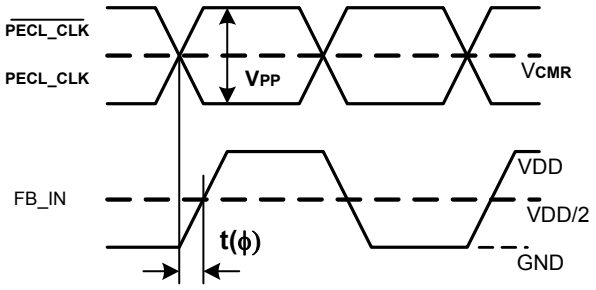


Figure 5. LVCMOS Propagation Delay t(ϕ), Static Phase Offset

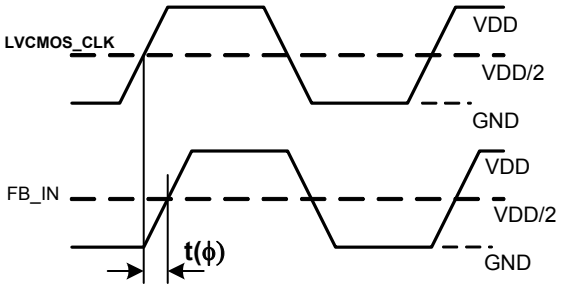


Figure 6. Output Duty Cycle (DC)

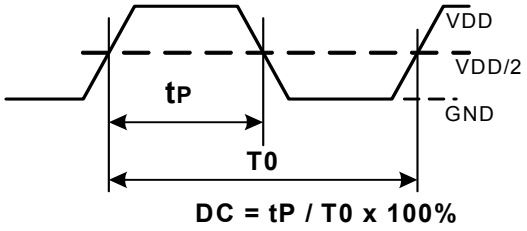
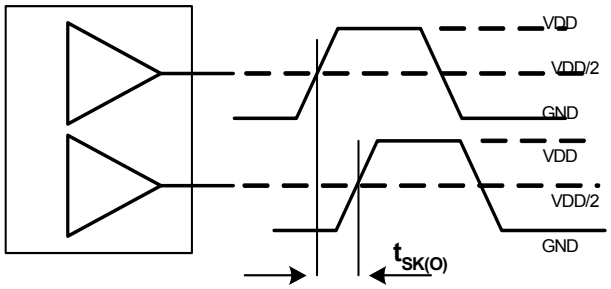


Figure 7. Output-to-Output Skew, $t_{sk(O)}$

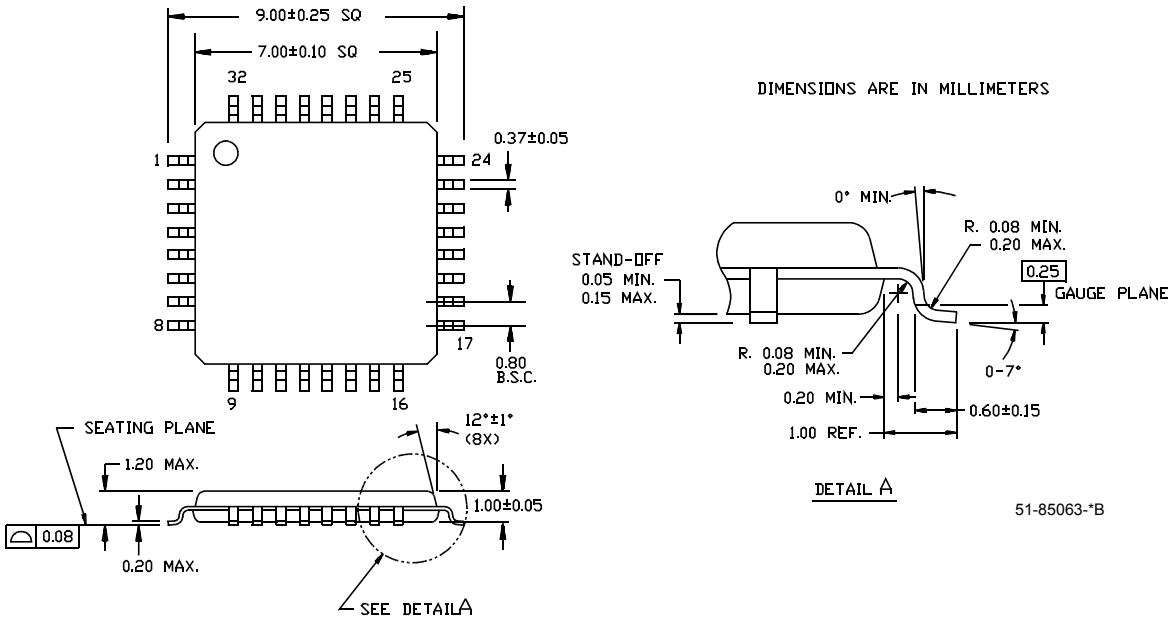


Ordering Information

Part Number	Package Type	Product Flow
Pb-free		
CY29351AXI	32-pin TQFP	Industrial, –40°C to 85°C
CY29351AXIT	32-pin TQFP – tape and reel	Industrial, –40°C to 85°C

Package Drawing and Dimension

Figure 8. 32-Pin Thin Plastic Quad Flatpack 7 x 7 x 1.0 mm



Document History Page

Document Title: CY29351 2.5V or 3.3V, 200 MHz, 9-Output Zero Delay Buffer Document Number: 38-07475				
REV.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	128152	RGL	07/07/2003	New Data Sheet
*A	245448	RGL	See ECN	Re-worded Select Function Descriptions in table 2.
*B	2001108	PYG/KVM/ AESA	01/23/2008	Corrected package thickness in Figure 7 from 1.4mm to 1.0mm. In Ordering Information, removed leaded and added Pb-free parts.
*C	2675313	KVM/PYRS	03/17/2009	Removed 'Preliminary' status Corrected typo in Document History Page

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